AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A semiconductor device, comprising:

a first metallization layer;

a first diffusion barrier layer disposed over said first metallization layer;

a first etch stop layer disposed over and spaced from said first diffusion barrier layer;

a dielectric layer;

a via extending through said dielectric layer, said first etch stop layer, and said first diffusion barrier layer; and

a sidewall diffusion barrier layer disposed on sidewalls of said via, said sidewall diffusion barrier layer formed by reverse sputtering of said first diffusion barrier layer, wherein said first diffusion barrier layer and said sidewall diffusion barrier layer are formed from a same material.

Claim 2 (Cancelled)

3. (Previously Presented) The semiconductor device according to claim 4, wherein said second etch stop layer includes silicon oxide.

4. (Currently Amended) A semiconductor device, comprising:

a first metallization layer;

a first diffusion barrier layer disposed <u>on and contacting</u> ~~over~~ said first metallization layer;

a second etch stop layer disposed on and contacting said first diffusion layer;

a first etch stop layer disposed on and contacting said second etch stop layer;

a dielectric layer disposed on and contacting said first etch stop layer;

a via extending through said dielectric layer, said first etch stop layer, said second etch stop layer and said first diffusion barrier layer, wherein said second etch stop layer has a thickness of at least 50 angstroms to about 120 angstroms.

Claims 5-6 (Cancelled)

Cont'd

7. (Previously Presented) The semiconductor device according to claim 1, wherein said material of said first diffusion barrier layer includes silicon nitride.

8. (Original) The semiconductor device according to claim 7, wherein said first diffusion barrier layer has a thickness of at least 50 angstroms.

9. (Previously Presented) The semiconductor device according to claim 1, further comprising a second diffusion barrier layer disposed over said sidewall diffusion barrier layer.

10. (Original) The semiconductor device according to claim 1, wherein said dielectric layer includes silicon oxide.

11. (Original) The semiconductor device according to claim 10, wherein said metallization layer includes copper.

12. (Original) The semiconductor device according to claim 10, further comprising a conductive plug disposed within said via, and wherein said conductive plug includes copper.

13. (Original) The semiconductor device according to claim 1, wherein the via has rounded corners

Claims 14-18 (Cancelled)

19. (Withdrawn) A method of manufacturing a semiconductor device, comprising the steps of:

depositing a first diffusion barrier layer over a first metallization layer;

depositing a dielectric layer over the first diffusion barrier layer;

etching the dielectric layer to form a via through the dielectric layer; and

sputtering the first diffusion barrier layer,

wherein said sputtering rounds corners of the via and deposits material of the first diffusion barrier layer onto sidewalls of the via to form a sidewall diffusion barrier layer.

20. (Withdrawn) The method of manufacturing a semiconductor device according to claim 19, wherein the first diffusion barrier layer includes silicon nitride.

21. (Withdrawn) The method of manufacturing a semiconductor device according to claim 20, wherein the first metallization layer includes copper and the dielectric layer includes silicon oxide.

22. (Withdrawn) The method of manufacturing a semiconductor device according to claim 19, further comprising the steps of:

depositing a second etch stop layer between the first barrier diffusion layer and the dielectric layer;

depositing a first etch stop layer between the second etch stop layer and the dielectric layer; and

etching the first etch stop layer after said dielectric etching.

23. (Withdrawn) The method of manufacturing a semiconductor device according to claim 22, wherein the second etch stop layer includes silicon oxide and the first etch stop layer includes silicon nitride.

Cont'd

24. (Withdrawn) The method of manufacturing a semiconductor device according to claim 19, further comprising depositing a second diffusion barrier layer over the sidewall diffusion barrier layer after said sputtering step.

25. (Withdrawn) The method of manufacturing a semiconductor device according to claim 24, further comprising depositing a conductive plug within the via.

26. (Withdrawn) The method of manufacturing a semiconductor device according to claim 25, wherein the conductive plug includes copper.

27. (Withdrawn) A method of manufacturing a semiconductor device, comprising the steps of:

forming a first metallization layer;

depositing a first diffusion barrier layer over the first metallization layer;

depositing a second etch stop layer over the first barrier diffusion layer;

depositing a first etch stop layer over the second etch stop layer;

depositing a dielectric layer over the first etch stop layer;

depositing a resist over the dielectric layer;

patterning the resist;

etching through the dielectric layer with a first etchant;

etching through the first etch stop layer with a second etchant; said etching of the dielectric layer and the first etch stop layer forming a via;

sputtering the first diffusion barrier layer, said sputtering rounding corners of the via and depositing material of the first diffusion barrier layer onto sidewalls of the via to form a sidewall diffusion barrier layer;

depositing a conductive material in the via over the sidewall diffusion barrier layer; and

planarizing a top surface of the dielectric layer.

28. (Withdrawn) The method of manufacturing a semiconductor device according to claim 27, wherein the first metallization layer and the conductive material include copper.

29. (Withdrawn) The method of manufacturing a semiconductor device according to claim 28, further comprising the step of depositing a second diffusion barrier layer over the sidewall diffusion barrier layer.

30. (Withdrawn) The method of manufacturing a semiconductor device according to claim 27, wherein the second etch stop layer includes silicon oxide and the first etch stop layer includes silicon nitride.